March 1988 Revised October 2000 74F841 10-Bit Transparent Latch

74F841 10-Bit Transparent Latch

General Description

The 74F841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 74F841 is a 10-bit transparent latch, a 10-bit version of the 74F373.

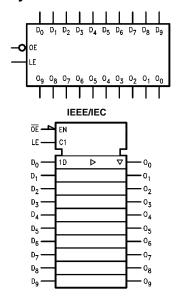
Ordering Code:

Order Number Package Number Package Description					
74F841SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide			
74F841SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide			
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.					

Features

■ 3-STATE output

Logic Symbols



Connection Diagram

ŌĒ —	1	\bigcirc	24	-v _{cc}
D ₀ —	2		23	-0,
D1 -	3		22	-0,
D ₂ —	4		21	_0,
D3-	5		20	-0 ₃
D4 -	6		19	_o₄
D5 -	7		18	-0 ₅
D ₆ -	8		17	-0 ₆
D ₇ —	9		16	-0 ₇
D ₈ -	10		15	-0 ₈
D ₉ —	11		14	— 0 ₉
GND —	12		13	-LE
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74F841

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OI}	
D ₀ -D ₉	Data Inputs	1.0/1.0	20 μA/-0.6 mA	
D ₀ -D ₉ O ₀ -O ₉ OE	3-STATE Outputs	150/40	–3 mA/24 mA	
OE	Output Enable Input	1.0/1.0	20 µA/–0.6 mA	
LE	Latch Enable	1.0/1.0	20 µA/–0.6 mA	

Functional Description

The 74F841 device consists of ten D-type latches with 3-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

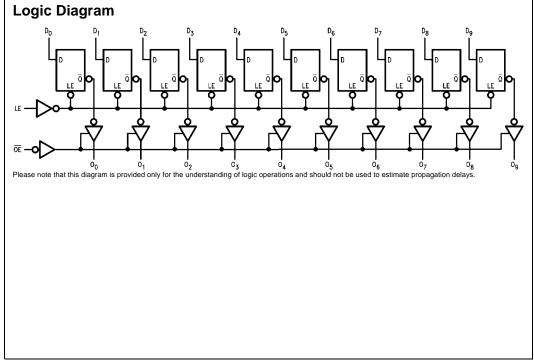
Function Table

I	Inputs		Internal	Output	Function	
OE	LE	D	Q	0	Function	
Х	Х	Х	Х	Z	High Z	
Н	н	L	L	Z	High Z	
н	н	н	н	Z	High Z	
н	L	Х	NC	Z	Latched	
L	н	L	L	L	Transparent	
L	н	н	н	н	Transparent	
L	L	Х	NC	NC	Latched	
L	Х	Х	н	н	Preset	
L	Х	Х	L	L	Clear	
L	Х	Х	н	н	Preset	
н	L	х	L	Z	Latched	
н	L	Х	н	Z	Latched	

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial Z = HIGH Impedance

NC = No Change



Absolute Maximum Ratings(Note 1)

Storage Temperature Ambient Temperature under Bias Junction Temperature under Bias V_{CC} Pin Potential to Ground Pin Input Voltage (Note 2) Input Current (Note 2) Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$) Standard Output 3-STATE Output Current Applied to Output -65°C to +150°C -55°C to +125°C -55°C to +150°C -0.5V to +7.0V -0.5V to +7.0V -30 mA to +5.0 mA

-0.5V to V_{CC}

-0.5V to +5.5V

Recommended Operating Conditions

Free Air Ambient Temperature Supply Voltage

0°C to +70°C +4.5V to +5.5V 74F841

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

in LOW State (Max) twice the rated I_{OL} (mA)

DC Electrical Characteristics

Symbol Parameter Min Тур Max V_{cc} Conditions Units Input HIGH Voltage 2.0 V Recognized as a HIGH Signal VIH Input LOW Voltage 0.8 ۷ Recognized as a LOW Signal V_{IL} Input Clamp Diode Voltage V_{CD} -1.2 V Min $I_{IN} = -18 \text{ mA}$ $I_{OH} = -1 \text{ mA}$ 10% V_{CC} 25 Output HIGH Voltage VOH 10% V_{CC} $I_{OH} = -3 \text{ mA}$ 2.4 V Min 2.7 $I_{OH} = -1 \text{ mA}$ $5\% V_{CC}$ 5% V_{CC} 2.7 $I_{OH} = -3 \text{ mA}$ V_{OL} Output LOW Voltage 10% V_{CC} 0.5 V Min I_{OL} = 24 mA $I_{\rm H}$ Input HIGH μΑ 5.0 $V_{IN} = 2.7V$ Max Current Input HIGH Current I_{BVI} 7.0 Max V_{IN} = 7.0V μΑ Breakdown Test I_{CEX} Output HIGH 50 μA Max $V_{OUT} = V_{CC}$ Leakage Current $I_{ID}=1.9\;\mu A$ V_{ID} Input Leakage 4.75 ٧ 0.0 All Other Pins Grounded Test Output Leakage $V_{IOD} = 150 \text{ mV}$ l_{OD} 3 75 μΑ 0.0 Circuit Current All Other Pins Grounded $V_{IN} = 0.5V$ Input LOW Current -0.6 mΑ Max $I_{\rm IL}$ Output Leakage Current Max $V_{OUT} = 2.7V$ 50 I_{OZH} μΑ Output Leakage Current -50 μΑ Max $V_{OUT} = 0.5V$ l_{ozl} Output Short-Circuit Current -60 -150 mΑ Max $V_{OUT} = 0V$ los Bus Drainage Test I_{ZZ} 500 μΑ 0.0V $V_{OUT} = 5.25V$ V_O = HIGH Z Power Supply Current 69 92 mA Max I_{CCZ}

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AC Electrical Characteristics

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Symbol			$T_{A} = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_{L} = 50 \text{ pF}$			$T_A = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$	
	Parameter						
	Parameter						
		Min	Тур	Max	Min	Max	1
t _{PLH}	Propagation Delay	2.5		8.0	2.0	9.0	ns
t _{PHL}	D _n to O _n	1.5		6.5	1.5	7.0	115
t _{PLH}	Propagation Delay	5.0		12.0	4.5	13.5	ns
t _{PHL}	LE to On	2.0		7.5	2.0	8.0	113
t _{PZH}	Output Enable Time	2.5		8.5	2.0	9.5	
t _{PZL}	OE to O _n	2.5		9.0	2.0	10.0	ns
t _{PHZ}	Output Disable Time	1.0		6.5	1.0	7.5	113
t _{PLZ}	OE to O _n	1.0		6.5	1.0	7.5	

AC Operating Requirements

		T _A = +25°C		$T_A = 0^{\circ}C$ to $+70^{\circ}C$		
Symbol	Parameter		$V_{CC} = +5.0V$		$V_{CC} = +5.0V$	
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	2.0		2.5		
t _S (L)	D _n to LE	2.0		2.5		
t _H (H)	Hold Time, HIGH or LOW	2.5		3.0		ns
t _H (L)	D _n to LE	3.0		3.5		
t _W (H)	LE Pulse Width, HIGH	4.0		4.0		ns

